2-Phase Sync Buck Switching Losses V1

This is a DEMO application schematic of a 2-phase synchronized rectified buck regulator using the SIMPLIS simulator. The nominal input voltage is 12V and the output voltage can be set to 1.0 V to 3.0 V. The purpose of this schematic is to study the switching losses in a synchronized rectified buck regulator.

This package also contains a generic multi-phase synchronous rectified buck PWM controller model for SIMPLIS. This is a voltage-model controller with a fixed switching frequency of 200 kHz for each phase. There is no fault latch-off for this controller. Instead, a cycle-by-cycle current limit is provided for the top MOSFET of each phase.

The generic multi-phase synchronous rectified buck PWM controller model is the same controller model as the one contained in the DEMO package for the multi-phase synchronized rectified buck regulator. There are several differences, however, in the set up of this schematic as compared to those schematics used for the multi-phase synchronized rectified buck regulator DEMO:

1. The MOSFETs in this schematic are set to use a higher-level of modeling. You can select each MOSFET, right click, and then left click “Edit Additional Parameters..,” to see that the modeling level is set to 1032. At this modeling level, all three capacitances of the MOSFET are modeled and the drain current is linearly controlled by the gate-to-source voltage after the gate-to-source voltage has exceeded the threshold.

   For the MOSFETs in the multi-phase synchronized rectified buck regulator DEMO schematics, the modeling level is set to 0001, which models the MOSFET as a switch plus gate-to-source capacitance. Modeling the MOSFET as switches plus gate gate-to-source capacitance, while adequate for the purpose of small-signal AC analysis and line/load transient analysis of the regulator, is not refined enough for the investigation of switching losses.

2. Source inductances have been added in the schematic. These source inductances were added to model the aggregate effect of the actual source impedance inside the MOSFETs and any connection parasitic inductances.

   In this simulation schematic, there is a damping resistor in parallel with each “source inductance” to model losses at the high frequencies.

3. Although the actual controller library file is the same as the one in the DEMO package for the multi-phase sync. buck regulator, the controller model used for the simulation here calls for output gate drivers that are more realistic compared to those that were used for the normal study of loop-gain AC analysis and input/output line transients.

   In the multi-phase synchronized rectified buck regulator DEMO schematics, the output gate drivers in the controller were modeled as ideal totem-pole switches. For the investigation of switching losses here, the output gate drives were

modeled as controlled current sources with finite rise and fall time, plus saturation.

4. To reduce the amount of CPU time required for the simulation, the schematic in this DEMO package is set up to run 2-phase operations only.

NOTE: Before opening the schematic, the simulation models for the PWM controller and the power MOSFETs, and the symbol for the PWM controller needs to be imported to your SIMetrix / SIMPLIS environment as they are not part of the standard release.

MultiPhase_SyncBuck.sxslb must be added as a symbol file to import the symbol of the PWM controller

The "MultiPhase_SyncBuck.sxslb" symbol file from this package contains the version-2 symbol of the generic multi-phase synchronous rectified buck PWM controller. If you have installed an earlier version of this symbol, please click the following sequence at the command-shell window of SIMetrix/SIMPLIS to remove the reference to the previous symbol file:

File | Symbol Editor | Symbol Manager | MultiPhase_SyncBuck.sxslb | Remove

Install the version-2 symbol of the generic multi-phase synchronous rectified buck PWM controller by clicking the following sequence at the command-shell window of SIMetrix / SIMPLIS:

File | Symbol Editor | Symbol Manager

In the Symbol Manager, click "Add" and browse through the directories to locate the MultiPhase_SyncBuck.sxslb file in this package and then click "Open."

MultiPhase_SyncBuck_PWM.lb must be added as a library model file

The "MultiPhase_SyncBuck_PWM.lb" library file from this package contains the version-2 model of the generic multi-phase synchronous rectified buck PWM controller. If you have never installed the model for this controller, or you have installed an earlier version of the model for this controller, you should use the Windows Explorer to copy and paste this library file into the "Models" directory located in the SIMetrix / SIMPLIS installation (root) directory.

Then both model and symbol must be associated

Click the following sequence at the command-shell window of SIMetrix / SIMPLIS:

File | Model Library | Associate Models and Symbols…

There is a square box on the left-hand side of the GUI. Click on it and scroll to select 4PHASE_SYNC_BUCK_CNTLR. If 4PHASE_SYNC_BUCK_CNTLR does not exist as a choice, then either the "MultiPhase_SyncBuck_PWM.lb" file was not properly deposited in the "Models" directory or the model/symbol associated has been carried out before. If you have carried out the model/symbol association for this controller earlier, you can skip the following instruction on association of model and symbol for the generic multi-phase synchronous rectified buck PWM controller.

If you were able to select 4PHASE_SYNC_BUCK_CNTLR, you will see a lot of text lines on the bottom half of the GUI, showing the content of the model for the PWM controller and the path name of the library file where it comes from. On the right hand side, click on the drop down list right under "Choose Symbol Category" to select "PSU controllers" and click the drop down list to the left of "New Symbol" to select 4PHASE_SYNC_BUCK_CNTLR. Then click "Apply Changes." Now the simulation model and the symbol for this generic PWM controller are associated and they would be ready for use in the schematics and simulation.

FDZ7064N.lb must be added as a library model file

Use the Windows Explorer to copy and paste this library file into the "Models" directory located in the SIMetrix / SIMPLIS installation (root) directory.
This file contains the SPICE simulation model for the FDZ7064N as obtained from the Website of Fairchild Semiconductor. The SIMetrix / SIMPLIS package will convert this model on the fly to the SIMPLIS model during simulation.

For more information, refer to the SIMetrix documentation.

The application schematic in this DEMO uses some advanced features in SIMetrix / SIMPLIS to handle parameterization. Such parameterization enables us to handily initialize a few components so as to expedite the computation of the periodic steady-state operation. You can bring up the schematic and run it as is without any modification. On the other hand, if you like to modify some of the component values, the output voltage, the load, or the number of phases involved, then you should read the Appendix at the end of this file before making any changes so that you would not, by accident, break up the parameterization.

There is only one simulation schematic for this DEMO package:

2_Phase_SwitchingLoss.sxsch – This test finds the periodic steady state operation using the POP analysis tool. After the analysis is finished, you can display the instantaneous power loss waveform of each component by the following in the schematic editor:

Click Probe | Power in Device…

Then click on the component you want to investigate the power loss.

While you are at the display tool, you can then click on the check box next to the name of the power loss waveform, and then click:

Measure | Mean

to obtain the average power loss of that component over the three complete switching cycles.

Appendix

The parameterization is accomplished by defining a set of variables and expressions in the text window of the schematics and by having the component values defined in terms of these variables. To open the text window, hit the F11 key in the schematic editor. You will see the following defined:

```
.VAR N_PHASE 2
.VAR VDC 1.5
.VAR ILOAD_MAX 80
.VAR LOAD_AT_t0 0.25
.VAR ILOAD_AT_t0 {LOAD_AT_t0*ILOAD_MAX}
.VAR IL_AT_t0 {ILOAD_AT_t0/N_PHASE}
.VAR RLOAD {VDC/(ILOAD_MAX*LOAD_AT_t0)}
.VAR DELTA_ILOAD {ILOAD_MAX*(1-LOAD_AT_t0)}
.VAR VCOMP_AT_t0 {1+2*VDC/12}
.VAR VC3_AT_t0 {VCOMP_AT_t0-VDC}
.VAR RILIM 27k
.VAR RDC_LOUT 1m
    .
    .
    .
```

You can edit the content here to change the number of phases of the regulated converter, the nominal regulated output voltage, the maximum load, the initial load, the resistance values for the four current limiting resistors, and the DC winding resistances for the four output inductors.

The command

```
.VAR N_PHASE 2
```

sets the number of phases to 2.

The command

```
.VAR VDC 1.5
```

sets the output voltage to 1.5 by setting the voltage reference VDAC to 1.5V. The voltage source VDAC is normally a VID signal. For the sake of simplicity, the VID control is replaced by a simple DC reference here in these DEMO schematics. You can set the nominal output voltage to any voltage between 1.0V and 3.0V.

The command

```
.VAR ILOAD_MAX 80
```

sets the maximum load current to 80A.

The command

.VAR LOAD_AT_t0 0.5

sets the initial load to 50% of the maximum load. The initial load sets the value of the equivalent load resistor used in the schematics.

The command

.VAR RDC_LOUT 1m

sets the DC winding resistances of the four output inductors to 1 milli-ohms.

If you like to change the component values for the following components:

output capacitor C1
compensation capacitor C3
the two output inductors L1 to L2
the two resistors RILIM1 to RILIM2 that set the current limit

you should select one of these components and hit the shift + F7 key combination instead of hitting the normal F7 key. This allows you to modify the component values without upsetting the link to the parameterization on the initial conditions. If you hit the F7 key to edit the component values on these components, you will get GUI dialogs to modify the values, but you will not be able to set the initial conditions to depend on the parameterizations. The component values of other components can be edited through the normal F7 key value dialog in SIMetrix.

You can change the peak current that triggers the cycle-by-cycle current limit by changing the component values of the four current limiting resistors RILIM1 to RILIM4. Each ILIM pin of the controller model draws 10 uA of current during normal operation. So the drain current of the upper MOSFETs at which the cycle-by-cycle current limit is triggered occurs at:

10^{-6} RILIM / Rds_ON

The default components in this DEMO schematic lead to a peak current limit of about 46A for each phase. Due to the source inductances modeled and the fact that the cycle-by-cycle current limit is achieved by comparing the voltages between the V12 and the MID1 and MID2 pins against the voltage drops across the current limiting resistors, the actual value at which the peak current limiting occurs is reduced because the normal di/dt in the output inductor L1 or L2 will cause a certain voltage drop across such source inductances. With the default components in this DEMO schematic, the peak current limit value is reduced to about 40A.